

Source: All Sources : Area of Law - By Topic : Patent Law : Patents : U.S. Patents : Utility Patents

Terms: patno is 5,777,391 (Edit Search)

*Pat. No. 5777391, **

5,777,391

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Jul. 7, 1998

Semiconductor device having an improved connection arrangement between a semiconductor pellet and base substrate electrodes and a method of manufacture thereof

REISSUE: Reissue Application filed Jul. 7, 2000 (O.G. Dec. 5, 2000) Ex. Gp.: 2815; Re. S.N. 09/613,541

INVENTOR: Nakamura, Atsushi, Fuchu, Japan
Nishi, Kunihiro, Kokubunji, Japan

ASSIGNEE-AT-ISSUE: Hitachi, Ltd., Tokyo, Japan (03)

APPL-NO: 570,646

FILED: Dec. 11, 1995

FOR-PRIOR:

Dec. 20, 1994 Japan 6-316444

May 25, 1995 Japan 7-126405

INT-CL: [6] H01L 23#49

US-CL: 257#778; 257#777; 257#780; 257#737; 257#784; 438#108; 438#617

CL: 257;438

SEARCH-FLD: 257#780, 777, 778, 737, 738, 697, 784; 438#108, 617

REF-CITED:

U.S. PATENT DOCUMENTS

5,107,328	4/1992	*	Kinsman	257#784
5,148,265	9/1992	*	Khandros et al.	257#695
5,422,435	6/1995	*	Takiar et al.	257#777
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5,677,566	10/1997	*	King et al.	257#778
5,684,330	11/1997	*	Lee	257#778

OTHER PUBLICATIONS

Nikkei electronics 1994.2.28 (No. 602), pp. 111-117. (with translation).

PRIM-EXMR: Thomas, Tom

ASST-EXMR: Hardy, David B.

LEGAL-REP: Antonelli, Terry, Stout, & Kraus, LLP

CORE TERMS: electrode, bonding, semiconductor, pellet, semiconductor device, electrically, mounting, slit, wire, rigid, substrate, resin, pad, conductor, bump, sealing, connecting, flexible, recess, through-hole, hole, modulus, molding, die, manufacture, thermal, coefficient, row, connect, deformed

ABST:

A semiconductor device comprising a semiconductor pellet mounted on a pellet mounting area of the main surface of a base substrate, in which first electrode pads arranged on the back of the base substrate are electrically connected to bonding pads arranged on the main surface of the semiconductor pellet. The base substrate is formed of a rigid substrate, and its first electrode pads are electrically connected to the second electrode pads arranged on its reverse side. The semiconductor pellet is mounted on the pellet mounting area of the main surface of the base substrate, with its main surface downward, and its bonding pads are connected electrically with the second electrode pads of the base substrate through bonding wires passing through slits formed in the base substrate.

NO-OF-CLAIMS: 25

EXMPL-CLAIM: 1

NO-OF-FIGURES: 16

NO-DRWNG-PP: 13

SUM:

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a method of manufacture thereof and more particularly to a technology effectively applied to a semiconductor device and a method of manufacture thereof, the device having a structure in which a semiconductor pellet is mounted on a pellet mounting area on the main surface of a base substrate and in which a first electrode pad on the back of the base substrate is electrically connected to an external terminal on the main surface of the semiconductor pellet.

A semiconductor device with a ball grid array (BGA) structure has been introduced as a semiconductor device having a high level of integration in the Nikkei Electronics, Feb. 28, 1994, pp. 111-117, published by Nikkei McGraw-Hill. The BGA structure of such as semiconductor device, as shown in FIG. 16 (cross section of an essential part), has a semiconductor pellet 2 mounted on a pellet mounting area of the main surface of the base substrate 1 and a plurality of bump electrodes 4 arranged in grid on the back of the base substrate 1 opposite the main surface.

The base substrate 1 may be made from a printed wiring board of two-layer wiring structure. Second electrode pads 1A are arranged in a peripheral area of the main surface of the base substrate 1 (around the pellet mounting area), while first electrode pads 1B are arranged on the back of the base substrate 1 opposite the main surface. The second electrode pads 1A are electrically connected to through-hole conductors 1C via conductors 1A1 arranged on the main surface of the base substrate 1. The first electrode pads 1B are electrically connected to the through-hole conductors 1C via conductors 1B1 arranged on the back of the base substrate 1.

The semiconductor pellet 2 may comprise mainly a semiconductor substrate 2B of single-crystal silicon. On the main surface of the semiconductor substrate 2B (device forming surface) is formed a logic circuit system, a memory circuit system or a combination of these. A plurality of bonding pads 2A are arranged on the main surface of the semiconductor substrate 2B. The bonding pads 2A are formed in the top of the interconnect layers formed on the main surface of the semiconductor substrate 2B.

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Ref	Items	Index-term
E1	1	PN=US 5777389
E2	1	PN=US 5777390
E3	1	*PN=US 5777391
E4	1	PN=US 5777392
E5	1	PN=US 5777393
E6	1	PN=US 5777394
E7	1	PN=US 5777395
E8	1	PN=US 5777396
E9	1	PN=US 5777397
E10	1	PN=US 5777398
E11	1	PN=US 5777399
E12	1	PN=US 5777400

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?s e3

S2 1 PN="US 5777391"

?t/39/

2/39/1

DIALOG(R) File 345:Inpadoc/Fam.& Legal Stat
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13227020

Basic Patent (No,Kind,Date): JP 8227908 A2 19960903 <No. of Patents: 002>

Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date
JP 8227908	A2	19960903	JP 95126405	A	19950525 (BASIC)
US 5777391	A	19980707	US 570646	A	19951211

Priority Data (No,Kind,Date):

JP 95126405	A	19950525
JP 94316444	A	19941220

PATENT FAMILY:

JAPAN (JP)

Patent (No,Kind,Date): JP 8227908 A2 19960903

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF (English)

Patent Assignee: HITACHI LTD

Author (Inventor): NAKAMURA ATSUSHI; NISHI KUNIHIKO

Priority (No,Kind,Date): JP 95126405 A 19950525; JP 94316444 A 19941220

Applic (No,Kind,Date): JP 95126405 A 19950525

IPC: * H01L-021/60

Derwent WPI Acc No: * G 96-452755; G 96-452755

Language of Document: Japanese

UNITED STATES OF AMERICA (US)

Patent (No,Kind,Date): US 5777391 A 19980707

SEMICONDUCTOR DEVICE HAVING AN IMPROVED CONNECTION ARRANGEMENT BETWEEN A SEMICONDUCTOR PELLET AND BASE SUBSTRATE ELECTRODES AND A METHOD OF MANUFACTURE THEREOF (English)

Patent Assignee: HITACHI LTD (JP)

Author (Inventor): NAKAMURA ATSUSHI (JP); NISHI KUNIHIKO (JP)

Priority (No,Kind,Date): JP 94316444 A 19941220; JP 95126405 A 19950525

Applic (No,Kind,Date): US 570646 A 19951211

National Class: * 257778000; 257777000; 257780000; 257737000; 257784000; 438108000; 438617000

IPC: * H01L-023/49

Derwent WPI Acc No: * G 96-452755

Language of Document: English

UNITED STATES OF AMERICA (US)

Legal Status (No,Type,Date,Code,Text):

US 5777391 P 941220 US AA PRIORITY (PATENT)
JP 94316444 A 19941220
US 5777391 P 19950525 US AA PRIORITY (PATENT)
JP 95126405 A 19950525
US 5777391 P 19951211 US AE APPLICATION DATA (PATENT)
(APPL. DATA (PATENT))
US 570646 A 19951211
US 5777391 P 19951211 US AS02 ASSIGNMENT OF ASSIGNOR'S
INTEREST
HITACHI, LTD. 6, KANDA SURUGADAI 4-CHOME
CHIYODA-KU, JAPAN ; NAKAMURA, ATSUSHI :
19951114; NISHI, KUNIHICO : 19951114
US 5777391 P 19980707 US A PATENT
US 5777391 P 20001205 US RF REISSUE APPLICATION FILED
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Continue: Y / N

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1/1 CRXX - (C) CLAIMS/RRX
AN - 3006688
PN - 5,777,391 A 19980707 [US5777391]
PT - E (Electrical)
PA - Hitachi Ltd JP
ACT - 20000707 REISSUE REQUESTED
Issue Date of O.G.: 20001205
Reissue Request Number: 09/613541
Examination Group responsible for Reissue process: 2815

UP - 2000-49
UACT- 2000-12-05

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1/1 PAST - (C) PAST
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PN - 5777391 A [US5777391]
DT - A (UTILITY)
OG - 2000-12-05
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ACT - REISSUE APPLICATION FILED
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Creation date: 10-24-2003
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Dossier: 09613541

Legal Date: 05-23-2001

No.	Doccode	Number of pages
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